

ABSTRACT

A method for fabricating an insulating layer having contact openings of varying depths for logic/DRAM circuits is achieved using a single mask and etch step. After forming stacked or trench capacitors, a planar insulating layer is formed. Contact openings are etched in the planar insulating layer to the substrate, and contact openings that extend over the edge of the stacked or trench capacitor top electrode, having an ARC, are etched using a novel mask design and a single etching step. This allows one to make contacts to the substrate without overetching while making low-resistance contacts to the sidewall of the capacitor top electrode. In the trench capacitor open areas are formed to facilitate making contact openings that extend over the top electrode. A series of contact openings that are skewed or elongated also improve the latitude in alignment tolerance.